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**A New Architecture for Single-Event Detection &
Reconfiguration of SRAM-based FPGAs**

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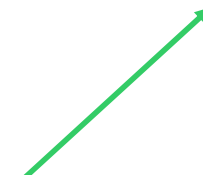
Outline

- ❑ Introduction
- ❑ Motivation for Proposed Architecture
- ❑ Xilinx Virtex Configuration Memory
- ❑ Prior Art
 - Triple Modular Redundancy (TMR)
 - Readback with Partial Reconfiguration
- ❑ Proposed Architecture
 - Concept, Dual-port SRAM, Error Detection Architecture and Sequence
- ❑ Simulation Results and Comparative Analysis
- ❑ Conclusion

Introduction

- Field Programmable Gate Arrays (FPGA) → in a variety of applications:
 - ranging from consumer electronics to devices in spacecrafts
 - flexibility of FPGAs in achieving requirements such as:
 - low cost,
 - high performance,
 - fast turnaround time
- SRAM-based FPGAs can experience single bit flips in the configuration memory due to
 - high-energy neutrons,
 - alpha particles hitting critical nodes in the SRAM cells.

Switching a bit
from 0 to 1
or 1 to 0.

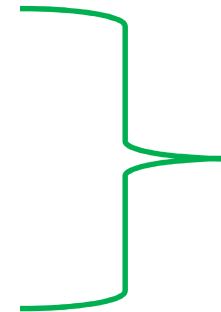


Introduction(2)

- High energy particles can be emitted by cosmic radiation or traces of radioactive elements in device packaging.
- The result could be
 - unwanted functional or
 - data modification
 - data loss in the system
- This phenomenon known as a Single Event Upset (SEU), and makes fault tolerance a critical requirement in FPGA design.
- For the dependability of the FPGA, it is paramount that the configuration bits are protected against faults such as Single Event Upsets (SEUs).

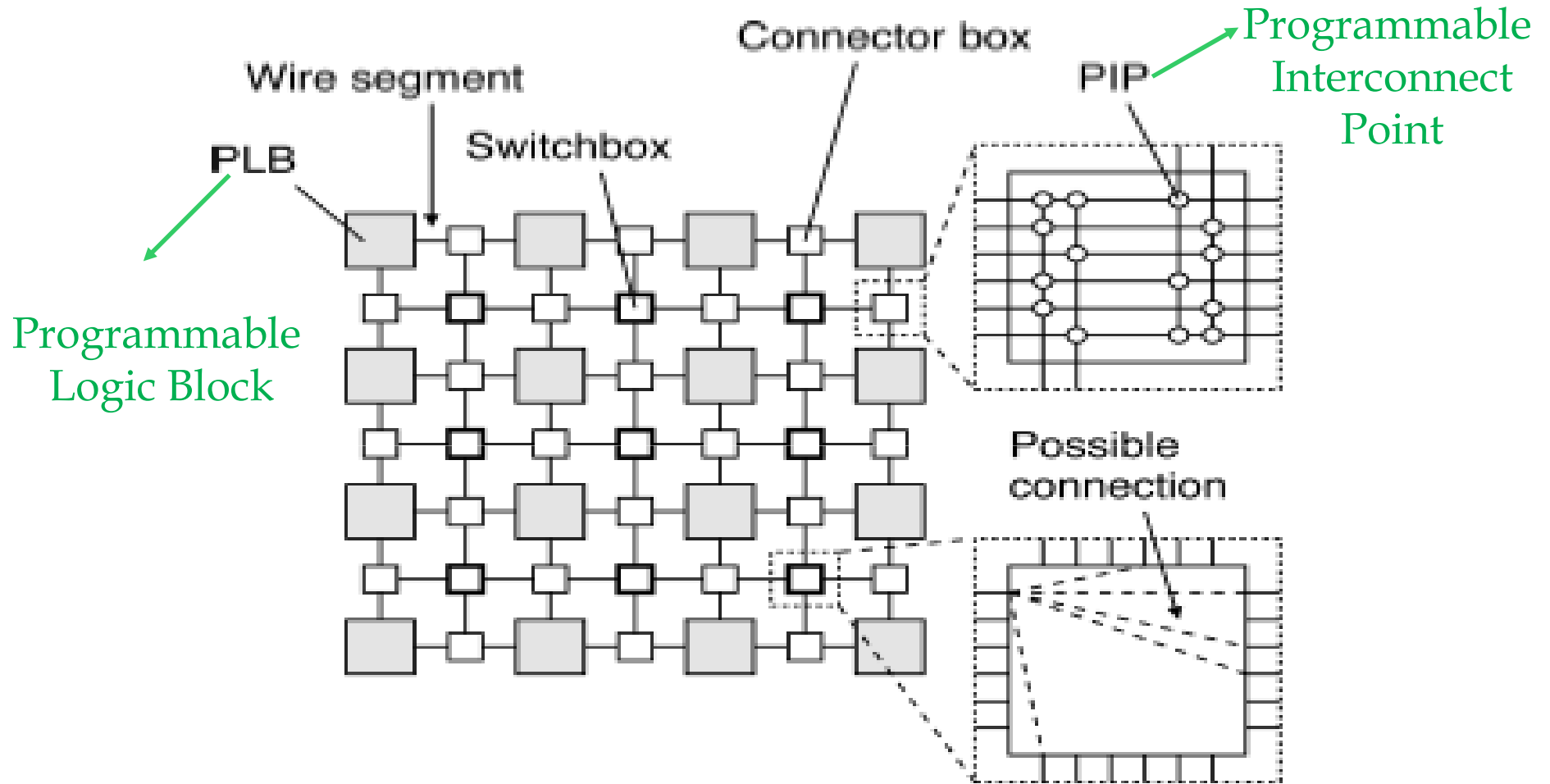
Introduction(3)

- SRAM-based FPGAs (from XILINX, Altera, Actel etc.)
 - store their configuration data stream in SRAM.
 - The configuration data control FPGA components such as:
 - the logic control blocks,
 - function look-up tables (LUT),
 - interconnect matrix and IO Blocks.
 - Two main configurable structures in an SRAM-based FPGA are:
 - look-up tables (LUT) and the routing multiplexers
- The entire functionality of the FPGA



The entire functionality of the FPGA

Introduction(4)



Generic FPGA architecture

Introduction(5)

- Configuration bits control the select lines of the routing multiplexers → a change in the configuration value could change the routing of a function being implemented !
- A change in the configuration bits of the LUT table → the entire function being implemented could be affected.
- For instance, a LUT implementing an *AND-gate* → implementing an *OR-gate*
- The effect of a fault in the sequential portion of the FPGA transient because the fault can be corrected in the next load of the latches.
- the combinational portion of an FPGA, upsets caused by flips in configuration bits first appear as transient faults, and then become permanent if the transient fault is latched by a storage cell, unless some detection and correction technique is applied.

Introduction(6)

- What's done in this study?
- Propose a shift in architecture from current SRAM-based FPGAs
- Architecture includes an inherent SEU detection through parity checking of the configuration memory.
- The inherent SEU detection sets a syndrome flag when an odd number of *bit flips* occur within a data frame of the configuration memory.
- To correct a fault, the FPGA is *partially reconfigured* without interrupting the normal operation of the FPGA device.

Introduction(7)

- What's done in this study?
- Existing solutions include:
 - Triple Modular Redundancy (TMR) systems
 - Readback and compare the configuration memory
 - Periodically reprogramming the entire configuration memory (scrubbing)
- The advantages afforded by the proposed architecture over existing solutions include:
 - Faster error detection
 - and correction latency over the readback method
 - Better area and power overhead over TMR.

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- **Conclusion**

Motivation for Proposed Architecture

- FPGAs are used in many critical applications:
 - in medicine
 - space research
- The effect of an SEU corrupting the configuration memory can sometimes be catastrophic.
- Principal purpose of this research is to find the optimal solution in designing single-event upset tolerant FPGAs.
- Existing solutions are effective but come at considerable costs of area, power and performance
- Any new solution proposed must improve on the existing methods

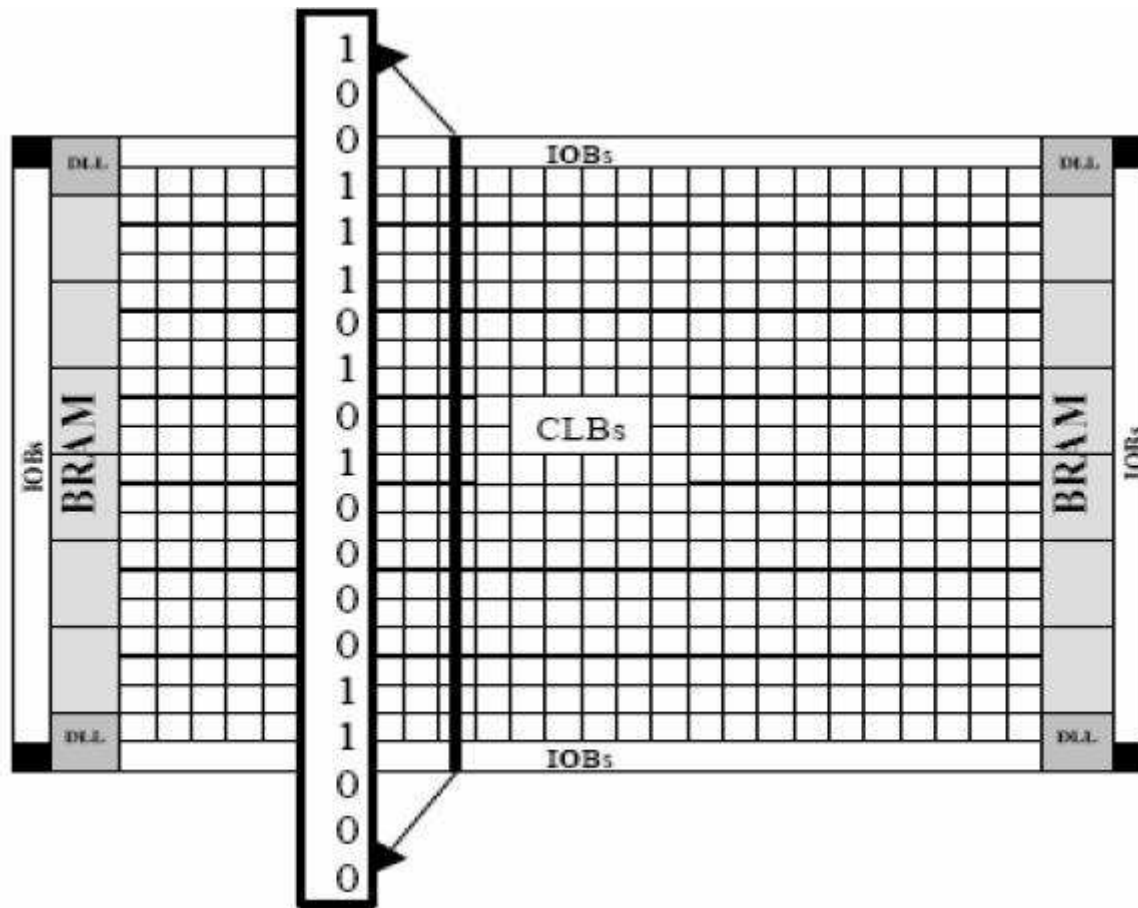
Motivation for Proposed Architecture(2)

- The critical constraints for the new SEU tolerant FPGA architecture :
 - It must not affect the normal operation of the FPGA.
 - It should have better power and area overhead over the TMR method
 - It should improve on the fault detection latency in readback method available in Xilinx Virtex FPGAs.
 - It must address the RAM access issues with Block RAMs during readback

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XILINX Virtex Configuration Memory



Xilinx Virtex FPGA Configuration Memory with illustration Data Frame

- Xilinx → leader in the FPGA industry
- They provide state-of-the-art devices.
- Configuration memory laid out in a regular pattern.
- The atomic component → data-frame. It is a 1-bit slice of the memory across its vertical axis.
- Configuration data stream is written to memory one data-frame at a time.
- Multiple frames make up a column and multiple columns make up the SRAM memory for the configuration layer.

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Prior Art

- A significant amount of research has been done in order to make FPGAs more *robust* and *fault tolerant*.
- These researches have led to a number of solutions and many proposed ideas in publications.
- The two most common solutions are:
 - 1. Method: Triple Modular Redundancy (TMR):
 - Voting the common output of three redundant modules of a design.
 - Xilinx Virtex FPGAs support TMR for mitigation of SEUs in designs
 - XTMR is a tool developed by Xilinx that automatically builds TMR into designs
 - The limitation of TMR in FPGA designs:
 - it triplicates the area required for a particular design
 - area increases → proportional increase in power consumption !

Prior Art(2)

- 2. Method: Readback with Partial Reconfiguration:
 - Continuously reading back content of configuration memory frame-by-frame, then performing a bit-by-bit compare with the original configuration bitstream stored in flash memory.
 - Error → the affected configuration frame is partially reconfigured with its original configuration bitstream
 - One drawback of this method is → not provide full coverage of all configuration data in the device. (readback is not a valid operation for blockRAM frames in Xilinx Virtex FPGAs.)
 - Another disadvantage → requiring three times the amount of system memory to function.
 - the original copy of the configuration bitstream must be available
 - a mask file is required to prevent false error reporting if the LUT frames are used as RAM
 - the readback data has to be stored while it is being compared

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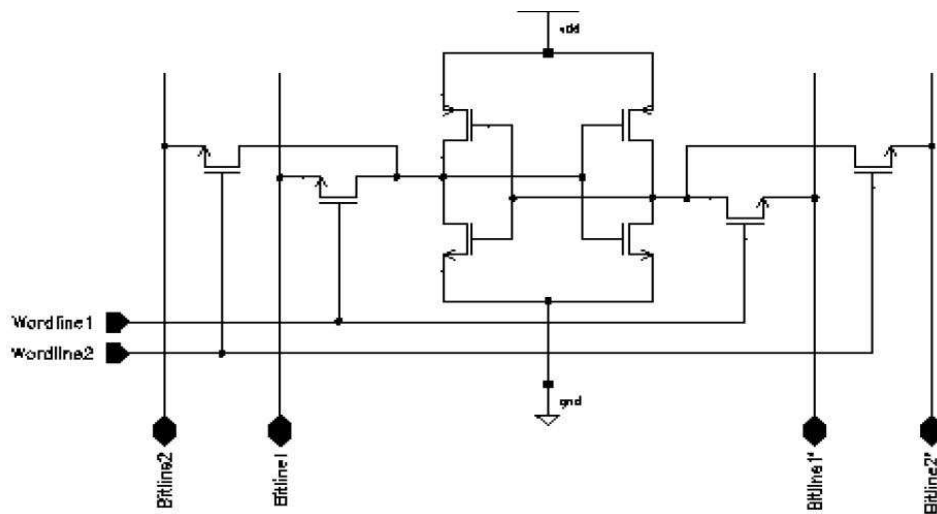
Proposed Architecture

➤ *Concept:*

- add parity trees to individual data frames of the configuration memory.
- If an odd-number of SEUs occur within that frame, then a syndrome flag for that particular frame is set. When a frame is affected, determined by a syndrome flag, it is partially reconfigured using the original bit stream for that particular frame.

➤ *Dual-port SRAM:*

➤ Modification of the SRAM cell



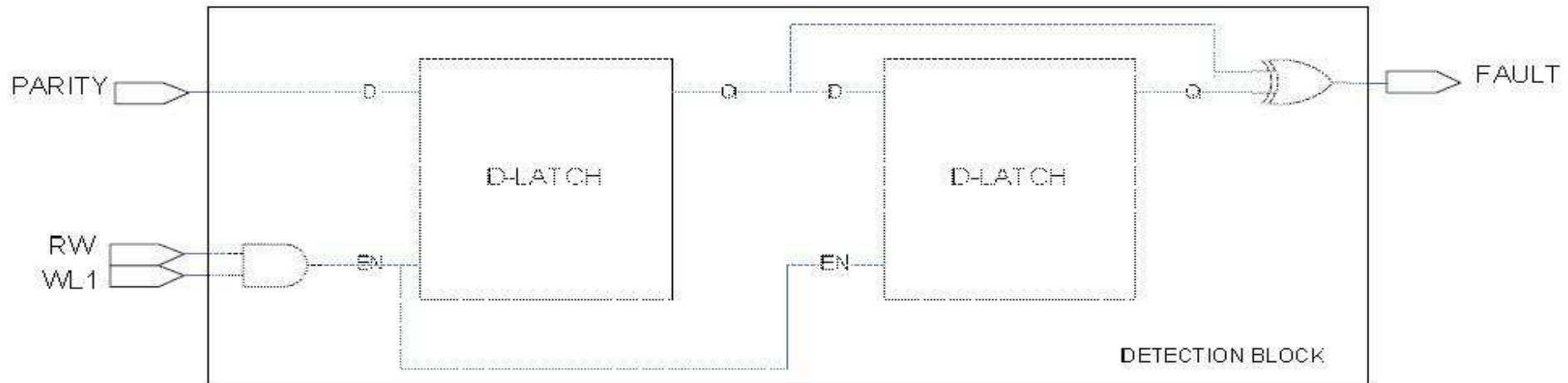
➤ Port-1 : responsible for normal FPGA functionality.

- configuration of its resources, partial reconfiguration and 'Readback' operations

➤ Port-2 : responsible for error checking and detection. It can only perform READ operations.

Proposed Architecture(2)

➤ Error Detection :



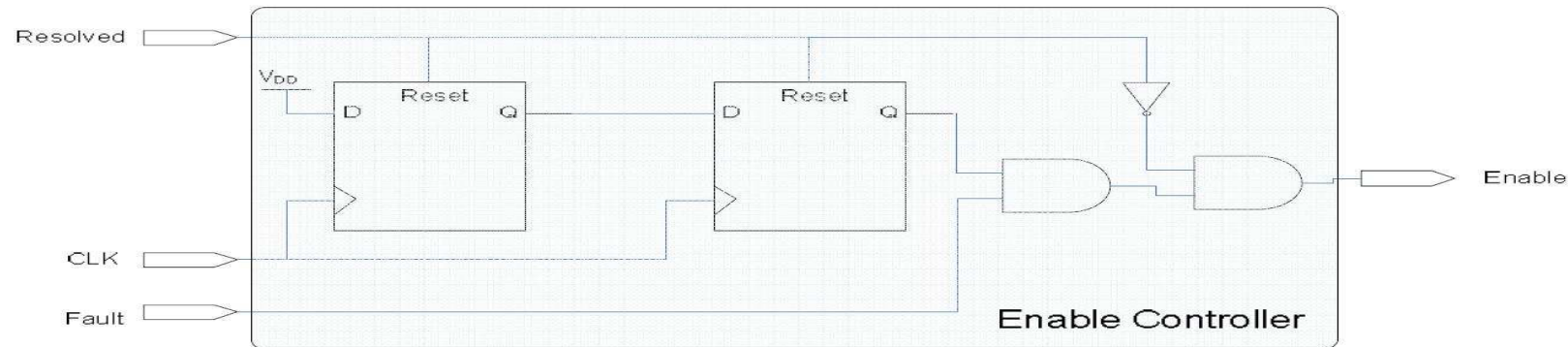
Error Detection Circuit

- Comparison of the current scan sequence parity bit and the latest previous scan parity value
- If the two values do not agree, then an odd number of bit-flips must have occurred in that frame.
- If the value in the first latch does not match that in the second latch, then the 'Fault' signal is set, indicating a SEU occurred in that frame.
- Each configuration frame would have its own dedicated error detection circuit.

Proposed Architecture(4)

➤ Error Detection Architecture and Sequence:

➤ Enable Controller:

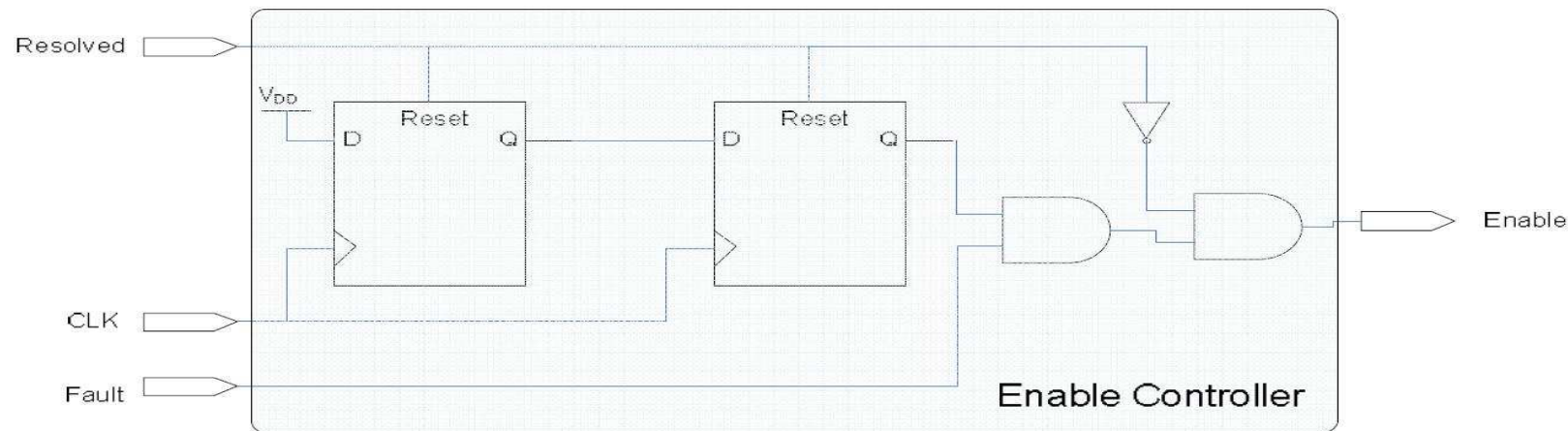


- Fault → Stop the scan sequence and trigger partial configuration.
- This controller enables or disables the addressing counter. Enables the counter (enabling the scan sequence) when :
 - *The system has stabilized after initial device/ partial configuration.*
- A “genuine fault” occurs when the output of the shift register is logic 1 and the fault signal is asserted. The enable signal is deasserted when a “genuine fault” occurs. This stops the counter and triggers partial reconfiguration.

Proposed Architecture(5)

➤ Error Detection Architecture and Sequence:

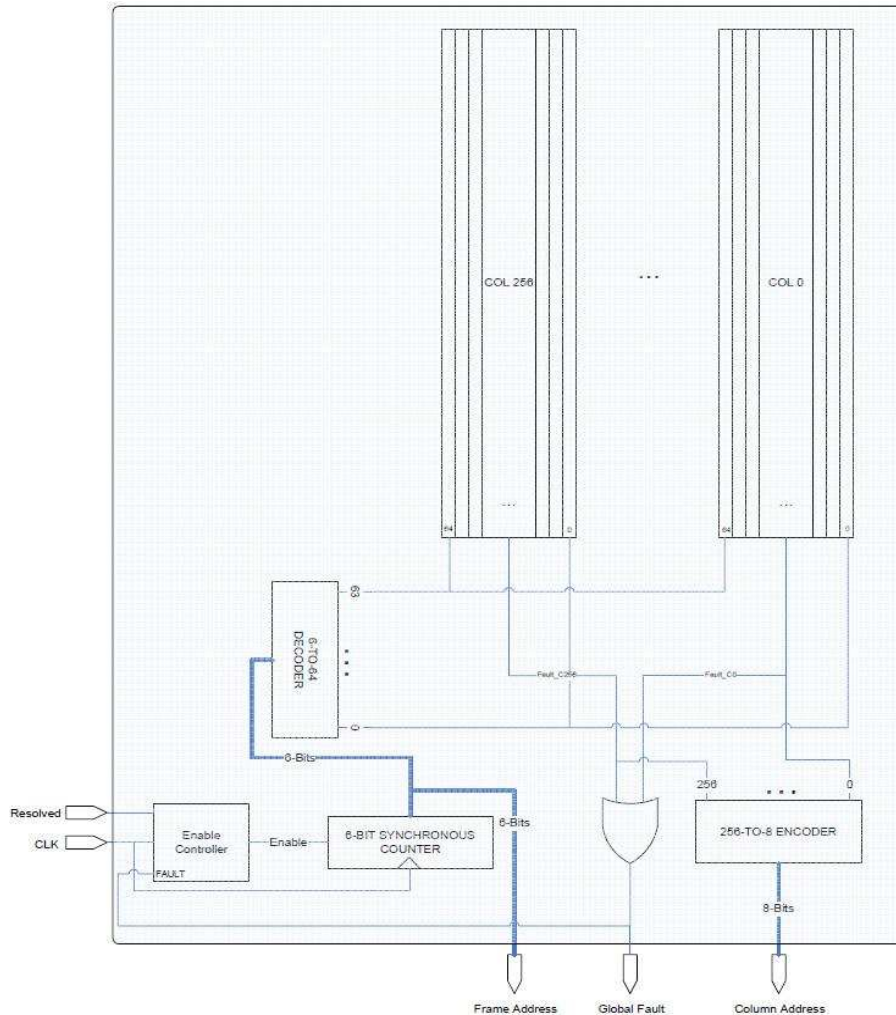
➤ Enable Controller:



- The enable signal becomes reasserted when the 'Resolved' signal is pulsed by the partial reconfiguration controller.
- The overall function of the enable controller is:
 - to stop the scan when a fault is detected and restart it after partial reconfiguration, determined by a pulse sent to the 'Resolved' signal.

Proposed Architecture(6)

➤ Error Detection Architecture and Sequence:

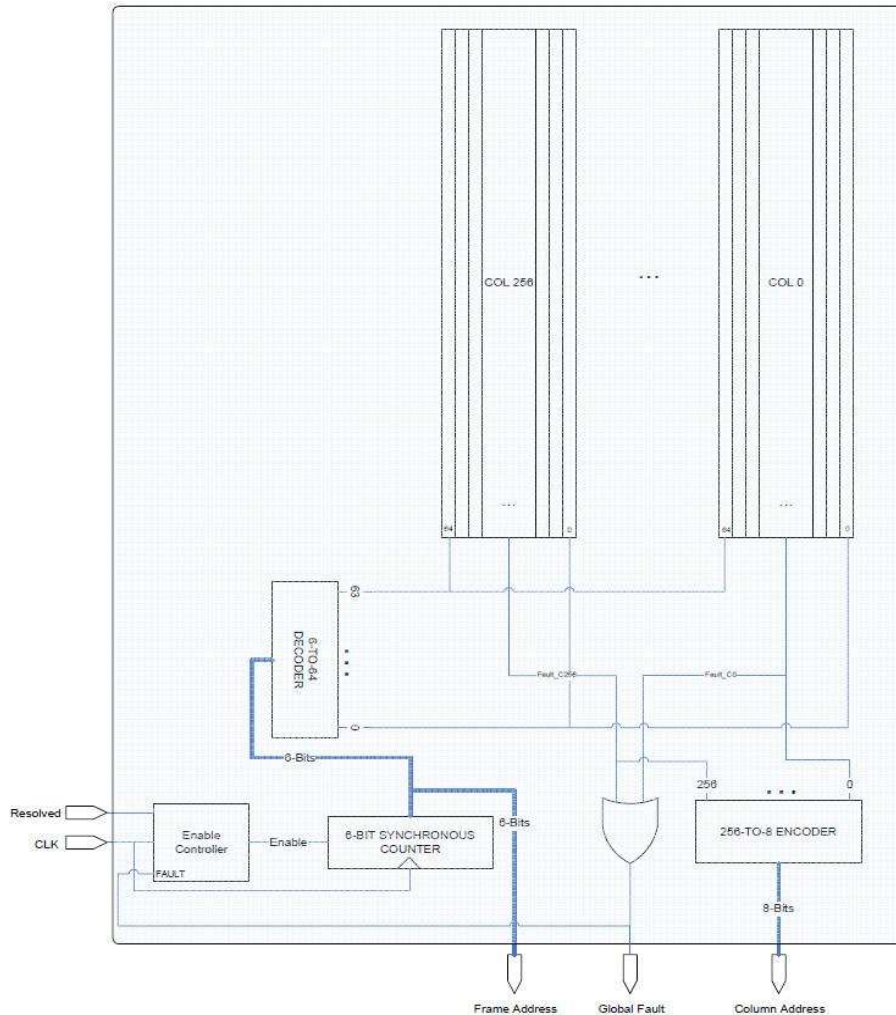


- Frame and Column Address
- Xilinx Virtex FPGAs uses a 'major' and 'minor' addressing
 - Major address → column in a config.
 - Minor address → frame within a col.
- Fig. → another illustration of the proposed architecture with multiple columns.
- Column address → determined by encoding the 'Fault Detected' signals of every column into an address in the fashion
- Frame address → current count of the synchronous counter when a fault is detected

Complete SEU Detection Controller

Proposed Architecture(7)

➤ *Partial Reconfiguration Controller:*



➤ inputs into this interface are:

➤ The 'Frame Address'

➤ The 'Column Address'

➤ the 'Global Fault' signal

➤ The output is the 'Resolved' signal → indicates partial reconfiguration has been completed.

Complete SEU Detection Controller

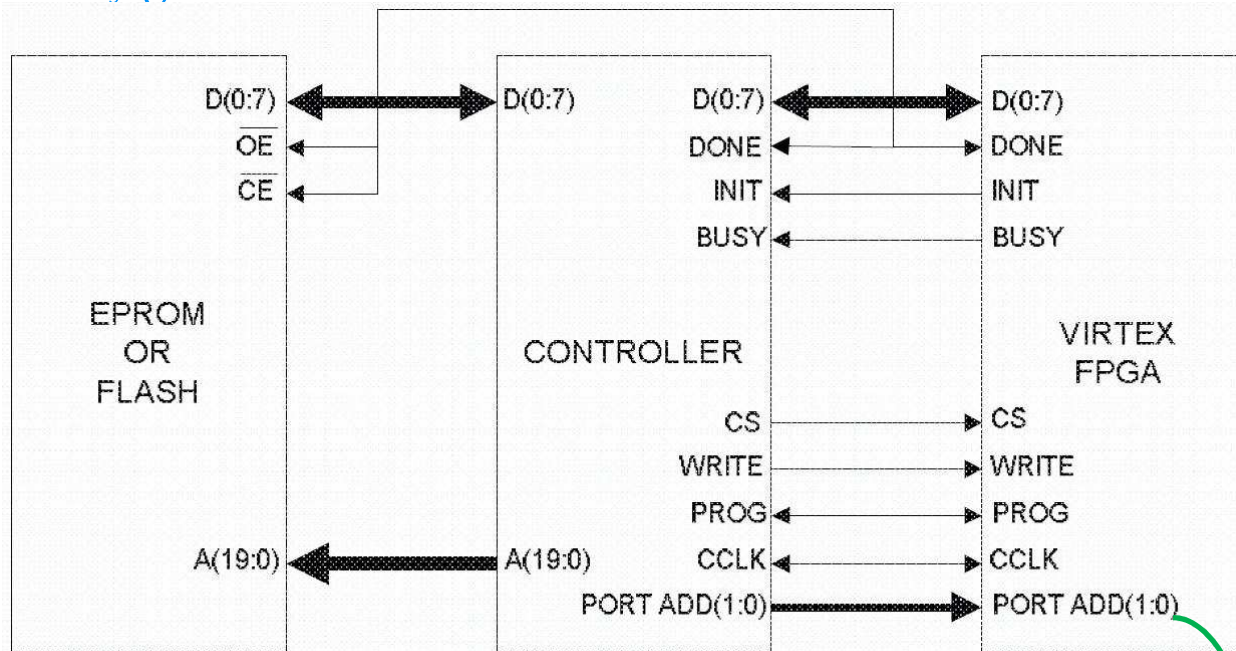
Istanbul, May 2009, Salih Bayar



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Proposed Architecture(8)

➤ Partial Reconfiguration Controller:



Device Interface through SelectMAP

PORT NAME	ADDRESS (2-BIT)
GLOBAL FAULT	00
COLUMN ADDRESS	01
FRAME ADDRESS	10
RECOVERED	11

The Port Address determines what device I/O port is being read or written

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Simulation Results & Comparative Analysis

- VHDL models of a
 - bare bone (without proposed modification) architecture
 - the proposed architecture
- Simulation → Mentor Graphic's 'ModelSim'
- Synthesize → Synopsys' 'Design Analyzer', (TSMC 0.35 um CMOS technology)
- Base device → the Xilinx Virtex XCV150
- The synthesis reports for the two set of models are compared in
 - Area,
 - Timing,
 - and Power.

Simulation Results & Comparative Analysis(2)

➤ 1. Area

UNIT	BAREBONE	PROPOSED	% INCREASE
SRAM Cell	225	474	110.67
SRAM Word	7225	16035	121.94
Frame	113044	256989	127.34
Controller + Miscellaneous	0	4137	N/A
XCV150	229366276	521434818	127.34

Summary of Percentage Increase in Area from Synthesis Report

- The percentage increase → the theoretical overhead that would be incurred if the proposed architecture is implemented.

Simulation Results & Comparative Analysis(3)

➤ 2. Timing

UNIT	TIME (NS)
SRAM Cell	0.73
SRAM Word	1.62
<i>Controller</i>	2.01
<i>or64</i>	1.96
<i>Encoder</i>	5.07
XCV150 Clock Period	12.48

- The minimum clock period required to accurately scan and detect faults is the information obtained from the Timing report

Critical Path Gate Delays from Synopsys Synthesis Tool for Proposed Architecture

Simulation Results & Comparative Analysis(4)

➤ 3. Power

UNIT	BAREBONE	PROPOSED	RATIO
SRAM Cell	20.85 μ W	41.68 μ W	1.999
SRAM Word	0.667 <u>mW</u>	1.36 <u>mW</u>	2.03
Frame	10.27 <u>mW</u>	21.76 <u>mW</u>	2.11

Power Dissipation Ratio of Bare Bone and Proposed Models

Simulation Results & Comparative Analysis(5)

➤ COMPARATIVE ANALYSIS

➤ 1) *Triple Modular Redundancy (TMR)*:

- The advantage of TMR over proposed architecture → there is no error detection latency (because faults are masked in TMR, it is therefore faster to “handle” an SEU with TMR than the proposed architecture)
- The disadvantages of TMR:
 - TMR has static fault coverage (while SEUs dynamic) : if SEUs at different times affect two modules of a TMR design → a permanent fault until the FPGA is reconfigured. (the conf. mem. refreshed as soon as an SEU occurs in proposed architecture)
 - A typical TMR design increases the area by approximately 200% due to the two redundant modules (only a 127% increase in area with the parity detection method)
 - TMR designs consume three times as much power as their Non-TMR counterparts (from 3.1 to 4.22 ratio, however a maximum 2.11 increase in power consumption for the proposed architecture)

Simulation Results & Comparative Analysis(6)

➤ COMPARATIVE ANALYSIS

➤ 2) *Readback with Partial Reconfiguration:*

- The advantage of 'Readback Method' over proposed architecture → the minimal increase in the FPGA device core area.
- The disadvantages of TMR:
 - 'Readback Method' triples the amount of system memory (A high end Virtex FPGA has over 16 million configuration bits → 16 MB of memory to store each one of the processing files.)
 - error detection latency is higher:
 - All frames are read sequentially for 'Readback Method'
 - Additional latency by the memory access time of the original bitstream file and the mask file in the 'Readback Method'
 - at 80 MHz and for Xilinx Virtex XCV150, a complete detection and correction sequence → **1.42 ms** for 'Readback Method', only **1.2 μs** for proposed architecture. (1000% imp. On error detection latency)

Simulation Results & Comparative Analysis(7)

➤ COMPARATIVE ANALYSIS

PROPERTIES	READBACK	TMR	PROPOSED METHOD
HARDWARE	200% Increase in System Memory	200% Increase in FPGA Configuration Memory	127% Increase in FPGA Configuration Memory
DETECTION LATENCY	1.42ms	N/A	1.2 μ s
DYNAMIC POWER DISSIPATION	Similar results as in "proposed method"	200% to 300% Increase in power. [15]	100% Increase in Power

Summary of Comparative Analysis of Proposed Architecture with Existing Methods

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Conclusions

□ Summary :

- ✓ Detecting and Correcting of Single event upsets (SEUs) in SRAM-based FPGAs with a new technique.
- ✓ Modifying configuration memory to become self-error checking.
- ✓ Dual-port SRAM configuration memory is used. (One port is dedicated to detecting SEUs through parity checking data frames.)
- ✓ Parity value of each data frame is compared with the parity from a previous scan. disagreement between the parity values → a syndrome flag is set to indicate the occurrence of an SEU in that frame
- ✓ The erring frame is corrected by *partial reconfiguration*. (without interrupting normal operation of the remaining portions of the system)
- ✓ Against the read-back and partial reconfiguration method
 - ✓ Improvement on the fault detection latency by over 1000%.
 - ✓ Reduce the amount of system memory required by 200%.
 - ✓ Improvement on area overhead of 37% over TMR (However, readback is superior in terms of hardware overhead).

References

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- ✓ F. Lima, L. Sterpone, L. Carro, M.Sonza Reorda, "On the Optimal Design of Triple Modular Redundancy Logic for SRAM-based FPGAs," 2005 IEEE
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For more references please see the original paper:

Eze Kamanu, Pratapa Reddy, Kenneth Hsu and Marcin Lukowaik "A New Architecture for Single-Event Detection & Reconfiguration of SRAM-based FPGAs", 10th IEEE High Assurance Systems Engineering Symposium (HASE 2007), 14-16 November 2007, Dallas, Texas, USA

Comments?

Questions?

Thank you for your attention!