

1. Solve the problem 7.77 from your book.
2. Show all synthesis steps in order to design following counter circuits, and write the VHDL code for your design. Your implementation should be component based. This means that flip-flops, multiplexers or any component except main gates (AND, OR, NAND, NOR, XOR, XNOR etc...) should be different components and used in the main circuit as a black box.
 - a) The counting sequence : 7 5 11 9
The state encoding type: Minimum binary
The flip-flop type: JK flip-flop
 - b) The counting sequence : 1 2 3 2 1 0
The state encoding type: Minimum binary
The flip-flop type: D flip-flop
 - c) The counting sequence : 5 6 6 7
The state encoding type: Direct binary
The flip-flop type: JK flip-flop